Chapter 12: The Cathodyne Phase Inverter

The cathodyne* is the quintessential phase inverter –beautifully simple and absolutely balanced when used properly. Fig. 12.1 shows a simplified cathodyne, and it can be seen that an inverted output is taken from the anode while a non-inverted output is taken from the cathode. It can be thought of as being half-way between an ordinary gain stage and a cathode follower, and provided the anode and cathode loads are exactly equal (including any external loads) we are guaranteed to get equal-but-opposite signal voltages developed across them, i.e. perfectly balanced outputs. This symmetrical loading leads to another popular name for the circuit –the **split load** inverter, while old texts may call it a **concertina** since the valve behaves like a concertina's bellows, alternately 'expanding' and 'contracting', i.e. decreasing and increasing its conduction to produce the output signals.

12.1: Design Equations

The outputs are 180° out of phase with each other because the anode current in each resistor is the same; if the current falls then the voltage drop across each resistor will fall, and therefore the anode voltage will rise while the cathode voltage simultaneously falls.

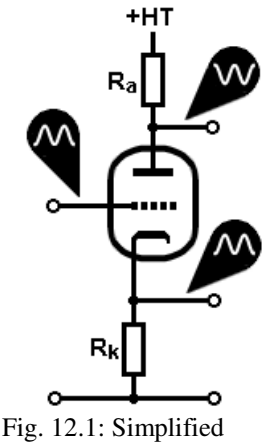


Fig. 12.1: Simplified cathodyne phase-inverter.

12.1.1: Gain

Since there are two outputs we have two ways of reckoning the gain. We could consider each output signal individually and then divide by the input voltage to get two figures for gain, one of which would be negative (inverting). Alternatively we could take the *total* output voltage measured *between* the two outputs, and divide by the input voltage to get a sort of overall measure of gain. This is called the **differential gain**; it is the difference between the individual gains to each output, taking sign into account.

Fig. 12.2 shows the transformation from the simplified circuit in into a Thévenin equivalent (remember, smoothing capacitor C_s is shown to remind you that HT and ground are shorted together as far as AC is concerned). The final step shown in fig. 12.2c deserves further comment. For a start, any external AC loads appear effectively in parallel with the load resistors R_a and R_k, so as they have been changed

* The name appears to be borrowed from a French amplifier circuit entitled 'Le Cathodyne', published in the early 1930s (The "Cathodyne", *Radio Review & Television News*, November 1932, p232). It actually featured an inverted gain stage Loftin-White, but was drawn in in such a way that it resembled the phase inverter now understood. It remains to be seen whether anyone saw the humorous allusion to the English word *anodyne* meaning harmless or dull!

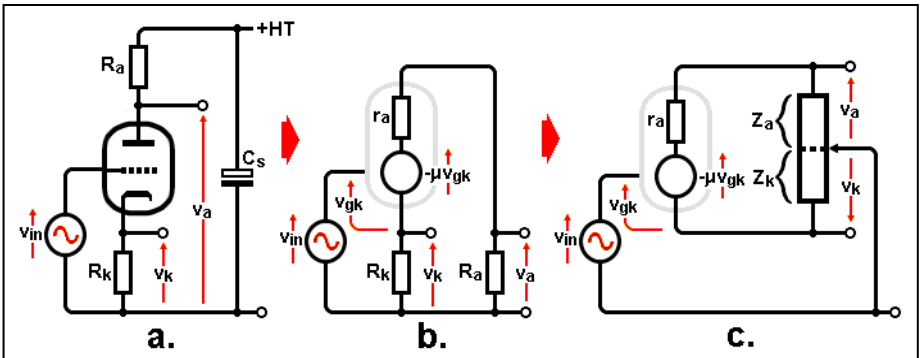


Fig. 12.2: Development of the Thévenin equivalent circuit of a cathodyne.

into generic impedances Z_a and Z_k to take this into account. More interestingly, they have been merged into a conceptual potentiometer whose wiper is grounded. This is to emphasise that the total differential output voltage is the voltage across the valve itself. If the 'wiper' were at the very top then the whole load impedance would be at the cathode and we would have a cathode follower with unity gain. If it were at the bottom then the whole load would be at the anode and we would have an ordinary gain stage with lots of (inverting) gain. By sliding the wiper along we morph between these two extremes, trading feedback for gain, and when it is at the centre-position the voltage is split exactly into two equal phases, that is, when –and only when– Z_a and Z_k are exactly equal.

For fig. 12.2 the two output voltages are quickly found using the formula for a potential divider:

$$v_a = -\mu v_{gk} \frac{Z_a}{Z_a + Z_k + r_a}$$

$$v_k = \mu v_{gk} \frac{Z_k}{Z_a + Z_k + r_a}$$

Noting also that $v_{gk} = v_{in} - v_k$, substitution and several steps of simplification lead to the following gain equations:

$$A_a = -\mu \frac{Z_a}{Z_a + r_a + Z_k(\mu + 1)} \qquad (12.1)$$

$$A_k = \mu \frac{Z_k}{Z_a + r_a + Z_k(\mu + 1)} \qquad (12.2)$$

These are exactly the same equations for the gain of a degenerated gain stage, and a cathode follower (with the extra impedance Z_a in series with r_a).

For the special case when $Z_a = Z_k = Z$ the equations become identical, i.e. the stage is perfectly balanced:

$$A = \pm\mu \frac{Z}{r_a + Z(\mu + 2)} \tag{12.3}$$

In most situations μZ will be much larger than r_a, so we can simplify one last time:

$$A \approx \pm \frac{\mu}{\mu + 2} \tag{12.4}$$

From the above we can see that the gain to each output will be close to unity, much like a cathode follower. The differential gain –measured between the two outputs– is therefore twice this figure, or about 6dB.

12.1.2: Output Impedance

The output impedance of the cathodyne has triggered heated debate in the pages of audio magazines for decades. It seems no matter how many times the issue is settled[1,2,3,4] (and it really is quite trivial) there are always newcomers who have not yet grasped it, and who start the debate again all over again. Some claim the output impedances of the anode and cathode are unequal and therefore the circuit is shamefully flawed, while others say the impedances are equal and the circuit is triumphantly perfect. Who's right? It turns out they both are, but as the parable of the blind men describing an elephant taught us, we need to look at the problem from more than one point of view.

Let us make no mistakes but skip the crux of the matter: a phase inverter has two outputs and therefore there are two ways to reckon its output impedance. The first way is to consider the impedance between either output and ground, individually, so we get two numbers. We will call these figures the **unbalanced output impedances**; they are the figures we would get by applying a test signal to each output *one at a time*, and using it to determine the impedance. We will skip the full analysis and apply some familiar maxims: when looking into the anode, anything below the cathode appears multiplied by $\mu+1$:

$$R_{o(a)} = \frac{R_a \left[r_a + R_k(\mu + 1) \right]}{R_a + r_a + R_k(\mu + 1)} \approx R_a \tag{12.5}$$

[1] Jones, G. E. (1951). An Analysis of the Split-Load Phase Inverter, *Audio Engineering,* December, pp16, 40-41.
[2] Peters, D. P. (1957). In Defense of the Split-Load Phase Inverter, *Radio & TV News*, November, pp182-4.
[3] Priesman, A. (1960). Notes on the Cathodyne Phase Splitter, *Audio*, April, pp22-3.
[4] Yaniger, S. (2010). Split the Difference: The Truth about the Humble Cathodyne, *Linear Audio*, 0, pp72-81.

When looking into the cathode, anything above it appears divided by μ+1:

$$R_{o(k)} = \frac{R_k (r_a + R_a)/(\mu+1)}{R_k + (r_a + R_a)/(\mu+1)} = \frac{R_k (r_a + R_a)}{R_k(\mu+1) + r_a + R_a} \approx \frac{2}{g_m} \qquad (12.6)$$

Hence we discover the unbalanced output impedance of the anode is much higher than that of the cathode, and this apparent discrepancy has prompted at least one designer to add a build-out resistor to the cathode to make its output impedance equal to that at the anode.[5] This is a mistake, however, as it actually makes the signal balance *worse*. This is why it is important to understand the other way of reckoning the output impedance.

The second way is to consider the impedance seen *between* the two outputs. We will call this the **differential output impedance**; it is a single number, easy to find by using the Norton equivalent circuit shown in fig. 12.3. By applying a fictitious test voltage v_1 between the outputs, a current i_1 flows back into the circuit and splits into i_2, i_3, and $g_m v_{gk}$. The first two are obviously given by $v_1/(R_a+R_k)$ and v_1/r_a. By further noting that $R_a = R_k = R$, then v_{gk} must be equal to $v_1/2$, so the last current must be $g_m v_1/2$. The output resistance is v_1 divided by all these currents, and we can eliminate v_1 by making it equal to one volt:

$$R_{o(diff)} = \frac{1}{\frac{1}{2R} + \frac{1}{r_a} + \frac{g_m}{2}} = \frac{2R \cdot r_a}{r_a + R(\mu+2)} \approx \frac{2}{g_m} \qquad (12.7)$$

However, at this point it is convenient to perform a conceptual sleight-of-hand by dividing this equation by two to get an **effective output impedance** for *each* output. These are the figures we would get if we applied *balanced* test signals to both

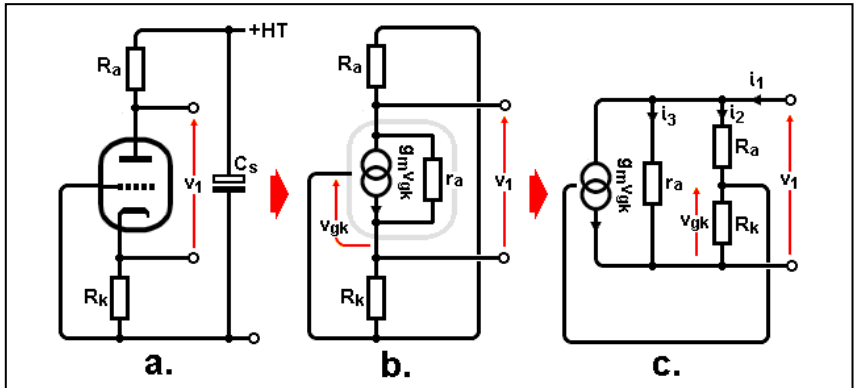


Fig. 12.3: Finding the output resistance of the cathodyne.

[5] Jones, M. (1996). A Fresh Look at Valve Power, *Electronics World*, January, pp24-8.

outputs *simultaneously*, and used them to measure the apparent output resistances of the anode and cathode:

$$R_{o(effective)} = \frac{R \cdot r_a}{r_a + R(\mu + 2)} \approx \frac{1}{g_m} \tag{12.8}$$

This is a very small figure, similar to a cathode follower. That such a small figure should apparently apply to the anode (it is identical to the cathode by definition) is surprising, hence the perennial discussion in audio literature. But all you need to remember is that the effective output impedances only apply *as long as the circuit remains balanced*.

These two different ways of reckoning output impedances serve two main purposes. If the cathodyne happens to be placed in a hum field, e.g. near a power transformer, then the hum picked up on the outputs depends on the *unbalanced* output impedances. In other words, we would find more hum at the anode (higher impedance) than at the cathode (lower impedance). For this reason the cathodyne is shamefully flawed when driving a balanced cable in a noisy environment – it needs to be buffered. On the other hand, if we are interested in the balance and bandwidth of the circuit then it is the *effective* output impedance that counts. As long as the outputs remain equally loaded, the output balance is perfect, and the bandwidth will be very wide since the effective output impedance is low (as confirmed by measurement in section 12.2.4). Thus as a phase inverter the circuit is triumphantly perfect – just don't expect it to drive unequal loads.

If for some reason the circuit becomes unbalanced then these effective output impedances will skew back towards equations 12.5 and 12.6. For the cathode the change is hardly significant, but for the anode it increases a great deal. The cathode output, therefore, is not affected much by changes in loading, but the anode is *strongly* affected by changes at either output.

12.1.3: Input Impedance

A full derivation of the complex input impedance of the cathodyne is quite tedious and unwieldy, so we will instead borrow some previous results. Since we have some gain to the anode (albeit not much) the Miller effect applies:

$$C_{ga}' = C_{ga}(1 + A_a) \tag{12.9}$$

Conversely, any impedance between grid and cathode will be bootstrapped by cathode follower action, as explained in section 7.1.2. We can therefore assert:

$$C_{gk}' = C_{gk}\frac{1 - A_k}{A_k} \tag{12.10}$$

Summing these two expressions and presuming $A_a = A_k \approx 1$, the total input capacitance is therefore:

$$C_{in} = C_{ga} + AC_{ga} + \frac{C_{gk}}{A} - C_{gk} \approx 2C_{ga} \tag{12.11}$$

This will typically be less than 10pF.

If a grid-leak resistance R_g is provided between grid and cathode then its apparent resistance will also be bootstrapped by cathode follower action. The approximate input resistance is the same as for a cathode follower (see the appendix for a derivation):

$$R_{in} \approx R_g \frac{A_k}{1 - A_k} \tag{12.12}$$

The result is likely to be several megohms.

12.1.4: PSRR

When looking at the anode of the cathodyne what we have can be viewed as a gain stage with a huge amount of cathode degeneration, so we can expect the PSRR of the anode to be very poor. However, when looking at the cathode what we have is more-or-less a cathode follower, so the PSRR of the cathode ought to be very good. This can be appreciated very easily by looking at the equivalent circuit from the point of view of the power supply, as shown in fig. 12.4. Remember from section 3.8.1 that when looking into the anode of an unbypassed gain stage we see the internal anode resistance r_a, plus the cathode resistor R_k, plus a sort of 'phantom' version of R_k which is multiplied by μ. From this figure it is easy to find the PSRR by applying the familiar formula for a potential divider, then turning it upside down. For the anode output:

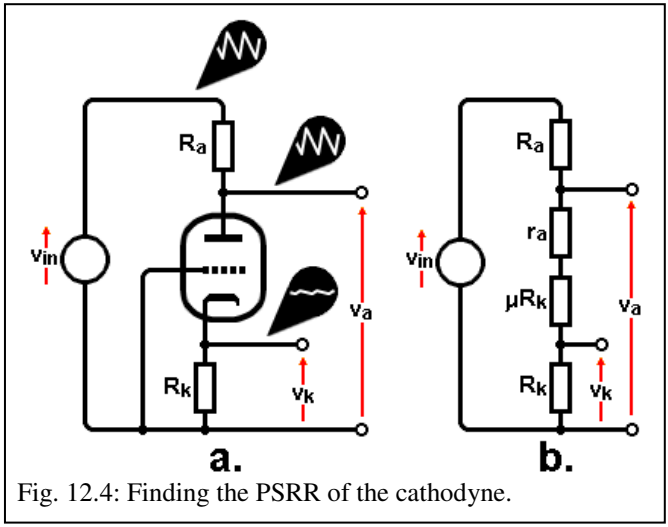


Fig. 12.4: Finding the PSRR of the cathodyne.

$$PSRR_a = \frac{R_a + r_a + R_k(\mu + 1)}{r_a + R_k(\mu + 1)} \approx 1 \tag{12.13}$$

For the cathode output:

$$PSRR_k = \frac{R_k}{R_a + r_a + R_k(\mu + 1)} \approx \mu \tag{12.14}$$

In other words, virtually all the power supply ripple will appear at the anode output, and hardly any at the cathode output. However, Broskie[6] points out that if half the HT ripple is deliberately fed forward to the cathodyne's grid, this ripple will be passed unnaffected to the cathode but appear inverted at the anode. It will therefore cancle out half the ripple already present at the anode, leaving *equal* ripple signals at both anode and cathode. These unwanted signals will then be rejected by the CMRR of the following stage (e.g. a push-pull power output stage). Fig. 12.5 illustrates how this could be achieved by arranging the preceding stage to have a PSRR of 6dB by making the dynamic resistance $r_{a1}+R_{k1}(\mu+1)$ equal to R_{a1} (the valves are shown direct coupled but this needn't be the case).

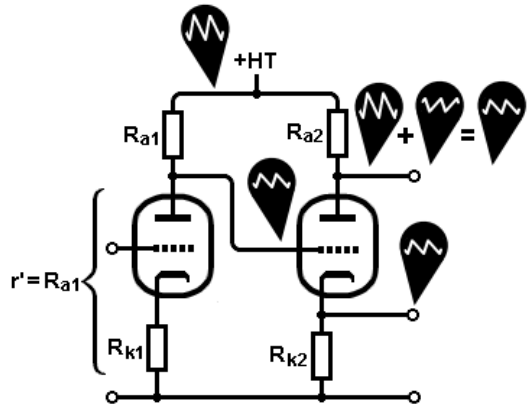


Fig. 12.5: The HT noise appearing at the cathodyne's outputs can be made equal (and in phase) by feeding approximately half the HT noise to the grid. The noise may then be rejected by the CMRR of a following stage.

Alternatively, it is worth pointing out that if the cathodyne is supplied from bipolar power supply rails with equal-but-opposite ripple on each, they will cancel, so ripple from both of the cathodyne's outputs will then be very small (but out of phase), as represented in fig. 12.6.

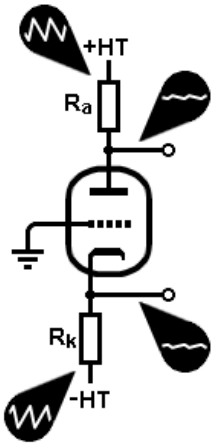


Fig. 12.6: With a bipolar supply the cathodyne's PSRR becomes symmetrical.

12.2: Designing a Cathodyne

Designing a cathodyne is somewhat similar to designing a cathode follower. The job of a cathodyne is easier, however, because we will not be using it to drive difficult loads. Normally it will either be driving a pair of power valves directly, or a pair of driver/buffer valves, as implied in fig. 12.7.

From our knowledge of load lines we know the output swing and linearity of a valve is maximised by using a large load resistance, but we also need to allow for any

[6] Broskie, J. http://www.tubecad.com/april99/page6.html

external AC load. This is particularly important for a phase inverter that drives power valves directly; it will need to deliver large signals to drive the output stage to full output and the AC load is likely to be fairly heavy since power valves cannot tolerate large grid leak resistances.

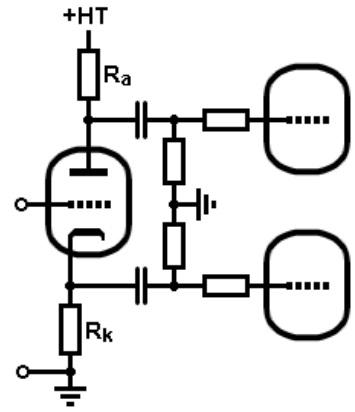


Fig. 12.7: The phase inverter usually has a predictable AC load consisting of grid leak resistors and Miller capacitance.

For example, a pair of 6V6GT beam-tetrodes in a typical class-AB output stage might be biased to around −20V, so each one will need a drive voltage of $20V_{pk}$ or $40V_{pp}$ for full output. Meanwhile, the grid leak resistors might be 100kΩ which is the datasheet maximum for fixed bias operation (500kΩ for cathode bias). Miller capacitance is likely to be around 25pF in pentode mode, 60pF in triode mode, or something inbetween for ultra-linear operation. With this information we can inch towards a suitable design for the phase inverter.

Since we are dealing with large signals we need to consider slew rate. Using the worst-case numbers, driving 20kHz, $20V_{pk}$ into a 60pF load requires a peak current of:

$$I_{pk} = 2\pi f V_{pk} C \quad = \quad 2\pi \times 20000 \times 20 \times 60 \times 10^{-12} = 151\mu A$$

To avoid slew limiting, the quiescent anode current needs to be greater than this. In this case the required current is tiny so there will be no difficulty here, but it is always worth checking. A load line can be now drawn for the cathodyne in exactly the same way as for any gain stage, remembering that it must represent the *total* load in series with the valve, $Z_a + Z_k$ (it is useful to learn to mentally 'flip-flop' between viewing individual outputs, and the total between the two outputs). For this example we will use an ECC81/12AT7 with a 300V HT. Yes, this triode has rather poor linearity, so it will be interesting to see how well it performs in a circuit with so much inherent feedback.

If the cathodyne is going to be driving 100kΩ grid leaks then we might choose load resistors of 22kΩ. The total DC load is therefore 44kΩ and a load line has been drawn in fig. 12.8. The AC load at each output is 22kΩ||100kΩ = 18kΩ, or 36kΩ total. The AC load line has been drawn through a tentative bias point of −3V, and the rotation of the load line is minimal.

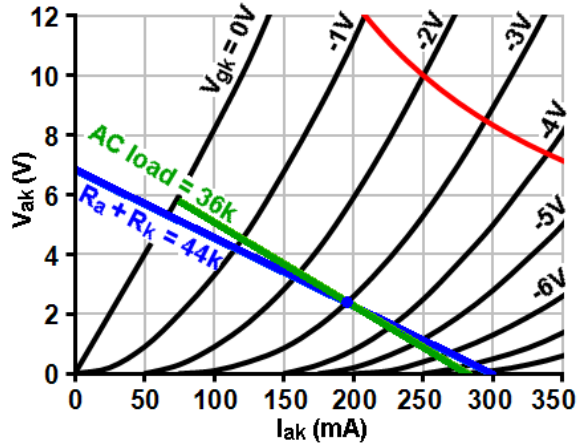


Fig. 12.8: DC and AC load lines for a cathodyne where $R_a = R_k = 22k\Omega$ and the following grid leaks are both 100kΩ.

Since the valve is biased to −3V it can swing symmetrically between the 0V and −6V grid curves. Reading off the AC load this would produce an output swing from 75V up to about 260V, i.e. a total signal swing of $185V_{pp}$. However, this will be divided equally between the two outputs, so the maximum swing from either one is in fact $92.5V_{pp}$. This is comfortably in excess of the $40V_{pp}$ that we actually need to drive each power valve, so headroom will not be a problem. What the load line does not tell us is the gain or linearity of the circuit. We cannot draw a new set of anode characteristics as we did for the cathode follower because now none of the valve electrodes remains at a fixed voltage. We could calculate gain using equation 12.3, but it is hardly worth the effort since we know automatically that it will be close to unity. All that remains is to bias the valve.

12.2.1: Cathode Bias

Unsurprisingly, the cathodyne can be cathode-biased just like any other stage. Indeed, the circuit can be viewed as an ordinary gain stage where half of the anode resistor has been sliced off and shoved underneath the circuit –this does not affect the value of bias resistor. However, we do need to be careful to keep the total load in the anode and cathode circuits equal at all times if perfect balance is to be ensured. Fig. 12.9 shows three ways this can be achieved. In each case R_g is the grid-leak resistor and will typically be 1MΩ, while R_1 is the precautionary grid stopper as usual.

The variation in fig. 12.9a is the one usually found in old circuits and textbooks. The cathode-bias resistor R_b is fully bypassed by a capacitor, C_k. This effectively shorts out R_b as far as AC signals are concerned, so the remaining loads are formed by R_a and R_k which are made equal. However, at low frequencies the circuit will become unbalanced as the reactance of C_k increases, causing the gain to the anode to fall. Fortunately, R_b is usually small and C_k is large, so any unbalance will be minimal and confined to sub-audio frequencies. These days R_b could be replaced with an LED which would eliminate this effect entirely.

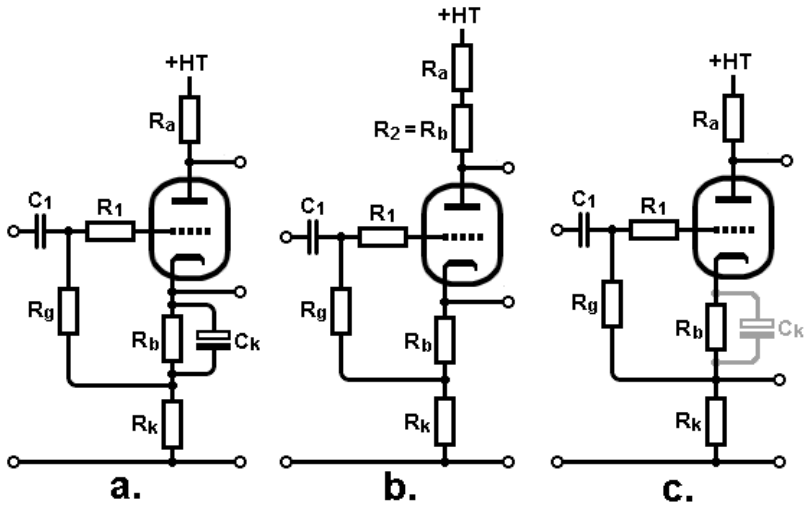


Fig. 12.9: Cathode-bias variations which maintain equal anode and cathode loading.

The version in fig. 12,9b ensures symmetry down to DC without resorting to an LED, by placing an extra resistor –equal to R_b– in the anode circuit, so the total load resistances are equalised. The electrolytic bypass capacitor is now redundant, which is always welcome.

The version in fig. 12.9c is a more subtle solution. Here the output has been moved from the top of R_b to the bottom so, as far as the AC equivalent circuit is concerned, the loads between each output and ground are simply R_a and R_k. AC balance is therefore ensured regardless of the presence of the bias network. Leaving R_b unbypassed will degenerate the valve's transconductance and so raise the output impedances and reduce the gain slightly, but this is unlikely to be significant so most designers would prefer to leave C_k out, or use a bias LED.

Whichever arrangement is used, the bias resistor R_b is found in exactly the same way as for a normal gain stage, either by drawing a cathode load line or by calculating its value from the bias point. Referring to fig. 12.8 the bias was –3V and the quiescent current was 2.3mA. The bias resistor would therefore be: 3V / 2.3mA = 1.3kΩ (this would also be a convenient value for the grid stopper –anything over $2/g_m$ will do). Fig. 12.10 shows how this circuit would look.

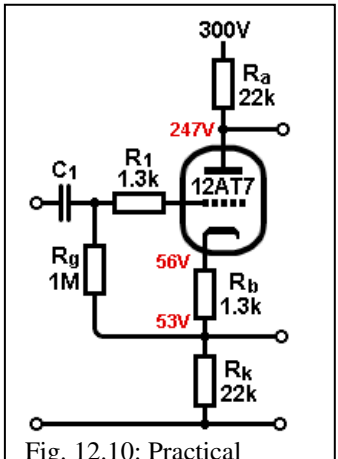


Fig. 12.10: Practical cathode-biased cathodyne.

However, we might not be satisfied with this circuit. For one thing, the input impedance varies wildly with frequency, from about 9.6MΩ at low

frequencies falling to less than 2MΩ at 20kHz, owing to the ~5pF input capacitance. What's more, R_g constitutes an unintended positive feedback path from cathode to grid, so the total amount of negative feedback within the circuit now depends on the source impedance (as explained for the cathode follower in section 7.5). The higher the source impedance, the lower the feedback fraction and therefore the higher the output impedance and distortion. To put it another way, R_g forms a bridge for unwelcome interaction between the previous stage and following stage. Such interaction may ultimately turn out to be minimal, but why suffer it at all? Fixed bias solves this problem with the same number of components.

12.2.3: Fixed Bias

Fixed-bias for the cathodyne is basically the same as for a cathode follower and need not be repeated in much detail (see section 7.6). The main difference is that the grid voltage for the cathodyne will be around half that of a cathode follower, because only half the DC load is now in the cathode circuit. Remembering the golden ratio from section 3.6.1, a resistor-loaded triode will typically be biased with about two-thirds of the total supply voltage across itself. The remainder appears across the load, which in this case is further divided between R_a and R_k. We should therefore expect the cathode and grid voltage of a simple cathodyne to be around one sixth of the HT.*

Fig. 12.11 shows the typical circuit arrangements for lifting the grid to the required voltage, either with a simple potential divider or by smoothing the bias voltage first with C_2. As explained for the cathode follower in section 7.6, the total (DC) grid-leak resistance for fixed biasing can be much larger than the maximum value given on the datasheet. This is because the heavy cathode-degeneration stabilises the circuit against grid current, so the grid-leak resistance can be A_o/A_{diff} times larger, where A_o is the open-loop gain (i.e. if the stage were reconfigured as an ordinary gain stage) and A_{diff} is the differential gain, which we know to be about 2. For example, under normal circumstances the 12AT7 would

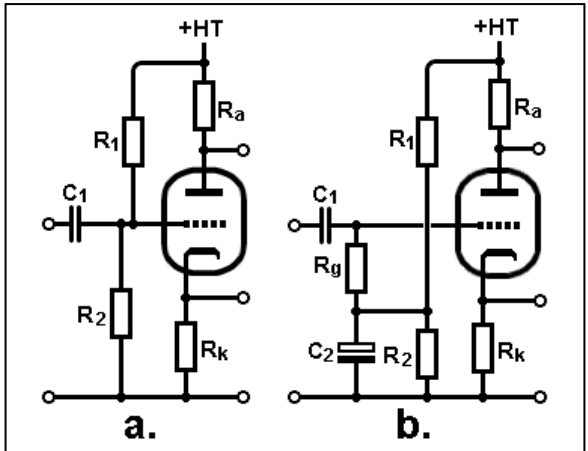


Fig. 12.11: Fixed-biased cathodyne (grid stoppers omitted for clarity). **a:** Simple arrangement; **b:** Decoupling the bias voltage using C_2.

* A transistor cathodyne (emitterdyne?) can swing almost rail-to-rail so would be biased with about half the supply voltage across itself, placing the base and emitter at around one quarter of the supply voltage.

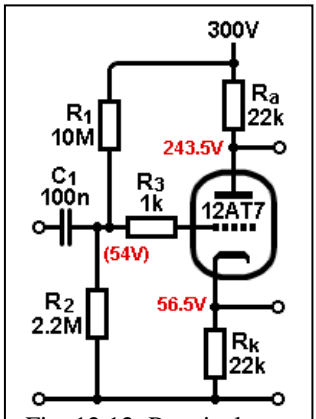


Fig. 12.12: Practical fixed-biased cathodyne.

provide a gain of about 40 with a 44kΩ load, so as a fixed-bias cathodyne we could make the grid leak resistance 40/2 = 20 times larger than normal – perhaps 20MΩ! This is almost certainly unnecessary of course; a few megohms is likely more than enough to satisfy the previous stage, whatever it may be, and very high node impedances should be avoided as they are sensitive to interference.

Continuing with the earlier example, fig. 12.8 showed the bias voltage was −3V and the quiescent anode current was 2.3mA. This current flows in R_k, so the cathode voltage will be 2.3mA×22kΩ = 50.6V. We want the grid to be 3V below this, or 47.6V. This is indeed about one sixth of the 300V HT and can be closely approximated with a 10MΩ/2.2MΩ divider, yielding 54V. The heavy cathode degeneration ensures the cathode will track the grid voltage, so we do not have to be very accurate (remember, you cannot measure the grid voltage with an ordinary voltmeter, owing to the high node impedance; measure the voltage *between* grid and cathode instead). Fig. 12.12 shows the final circuit with actual measured voltages –the bias turned out to be −2.5V.

12.2.4: Measured Results

The circuit described above was first tested for frequency response –the thing that has misled so many designers in the past. The two outputs were coupled to a dual-channel oscilloscope with short, identical cables, so the total load on each amounted to 1MΩ||40pF. To swamp any mismatch and to make the bandwidth easier to measure, an additional 470pF load capacitor was then added to either output, or to both. The input was supplied with a $0.5V_{pk}$ sinewave as this allowed testing up to 1MHz without slew-rate limiting –an easy point to forget when testing at such high frequencies. Fig. 12.13 shows

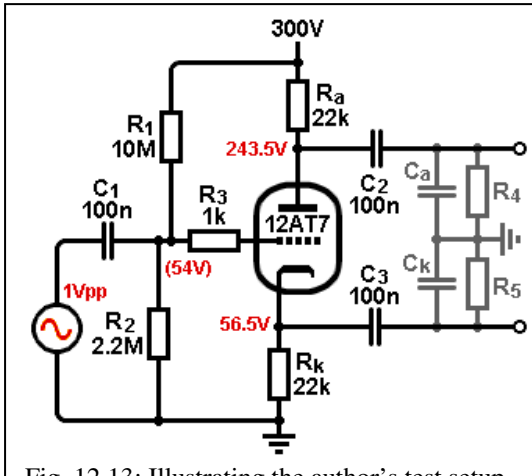


Fig. 12.13: Illustrating the author's test setup. To measure bandwidth, R_4/R_5 represent the 1MΩ input resistance of the oscilloscope. C_a/C_k represent 40pF cable and input capacitance, or 510pF deliberate load capacitance. To measure output impedance, R_4/R_5 were switched between 1MΩ and 10kΩ.

the test setup more clearly. Remember, the two outputs were monitored simultaneously.

The upper graph in fig. 12.14 shows the result when the anode is loaded with only 40pF while the cathode sees the heavier 510pF. C_k now acts like a small cathode bypass capacitor, causing a gain boost at high frequencies when looking at the anode, making the circuit appear ridiculously unbalanced.

The middle graph in fig. 12.14 shows the result when the capacitive loads are swapped. The bandwidth as measured at the anode is now very poor owing to its high output resistance, but from the cathode it is very wide. A similar effect would be seen if the outputs were measured one at a time so only one output sees the capacitive load of the measuring equipment at any time. This is why so many designers have been tricked into thinking the cathodyne is flawed at high frequencies.

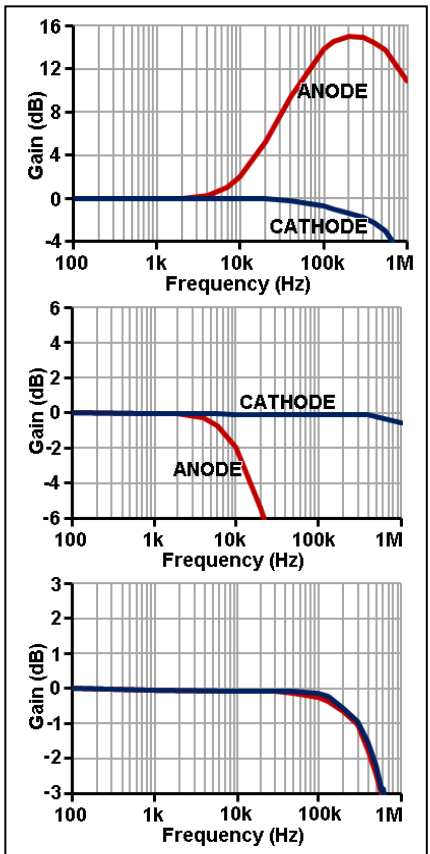


Fig. 12.14: Frequency response of the circuit in fig. 12.13.
Upper: C_a = 40pF, C_k = 510pF;
Middle: C_a = 510pF, C_k = 40pF;
Lower: C_a = 510pF, C_k = 510pF.

The lower image in fig. 12.15 shows the result when both outputs are equally loaded –as they are (or should be) during normal operation. To our relief the theory is confirmed; the two outputs are practically identical, the tiny variation being due to small differences in the capacitances. The −3dB point was determined to be 595kHz implying an effective output resistance of 525Ω. Of course, in actual use the cathodyne would not be loaded with such large capacitances, so the bandwidth would in fact extend breezily into the megahertz region. Also note that the low-frequency gain is extremely close to unity (×0.944 to be exact). This is about as close to perfect as any simple circuit gets!

If further confirmation were needed, the output resistances were also measured directly. With the input increased to $10V_{rms}$ 1kHz, the outputs were both noted to be 9.44V. When only the anode output was loaded with 10kΩ, the anode output dropped to 3.0V indicating an output resistance of 21kΩ. Swapping the loading, the cathode signal dropped to 8.56V, implying 1kΩ output resistance. But with both outputs loaded simultaneously, both outputs fell to 8.96V indicating effective output

resistances of 530Ω. A closer match to the figure derived above could hardly be asked for.

Before going on, it is worth mentioning that by temporarily using a 100kΩ grid stopper the –3dB frequency fell to 252kHz, implying 6.3pF input capacitance. Also, fig. 12.15 shows the distortion performance measured at the two outputs using the method outlined in chapter 6. The two traces are of course identical, low, and not very interesting, since the signal analyser can only deliver about $13V_{rms}$ maximum –nowhere near the circuit's overload limit. Remember, the rise at low levels is the noise floor, not distortion. Fig. 12.16 shows the distortion spectrum at $10V_{rms}$ output (the fundamental has been nulled out by the analyser).

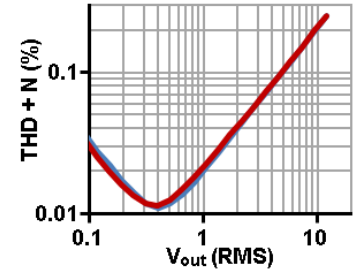


Fig. 12.15: Distortion performance of the circuit in fig. 12.13 at 1kHz.

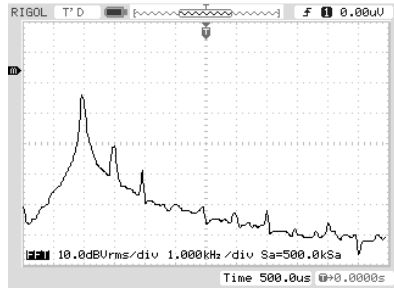


Fig. 12.16: Distortion spectrum for the circuit in fig. 12.13 at 1kHz, $10V_{rms}$.

Since there are two triodes in the bottle, let's make things a little more plausible by adding a preceding gain stage. Fig. 12.17 shows the circuit chosen. V_2 is unchanged while V_1 is arranged as a simple gain stage with component values chosen so several valve types can be plugged in without adjustment. R_{g1} simulates a typical source resistance. Since a degenerated circuit rather similar to this was already tested in section 7.10, V_1 has been fully bypassed here for variety (indeed, if R_{a1} was made equal to R_{k2} then the pair would form a constant-current-draw amplifier as described in section 7.10). The HT was reduced to 250V for the less hardy valve types.

Fig. 12.17 also shows the distortion measured at the cathode output, the anode output being identical of course. In every case the spectrum was almost pure second harmonic as usual, and not worth presenting. Table 12.1 summarises the operating conditions (it is left as an exercise for the reader to work out the operating currents), and the ECC88 is clearly the winner in terms of absolute distortion. However, if we take gain/distortion as a figure of merit (since this would allow more distortion reduction if feedback were applied) then the 12AX7 would win, despite the rather low-impedance loading, while the 12AU7 and ECC804 would rank worst-equal.

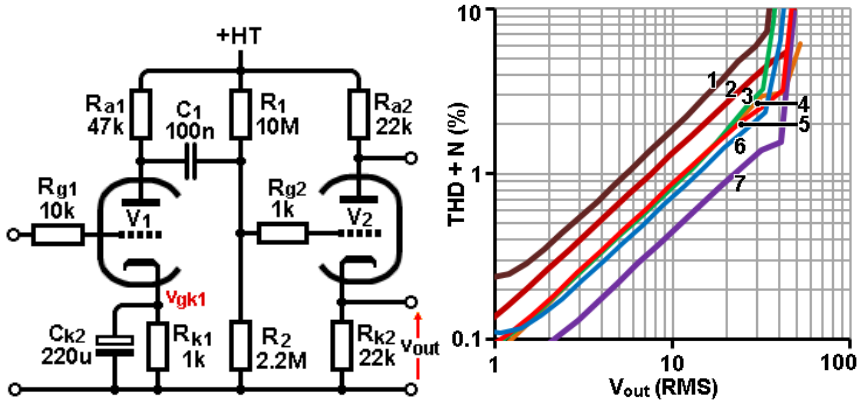


Fig. 12.17: **Left:** Practical gain stage / cathodyne pair for analysis. **Right:** Distortion versus level at 1kHz with various different valves. Refer to Table 12.1.

Trace	Type	HT	V_{gk1}	Total Gain
1	6H2П-EB / 6N2P-EV	300V	1.6V	47.2
2	Sovereign 12AT7WA	300V	2.5V	40.3
3	Sovtek 12AX7LPS	300V	1.6V	51.8
4	Sovereign 12AU7WA	300V	3.8V	14.3
5	Mazda ECC804	250V	3.4V	14.6
6	6H1П-ВИ / 6N1P-VI	250V	2.5V	28.5
7	Mullard ECC88	250V	3.1V	26.9

Table 12.1: Figures relating to fig. 12.17.

12.2.5: DC Coupling

The cathodyne is an obvious candidate for DC coupling, although things are not as simple as they were for the cathode follower because now the required grid voltage is so much lower. This makes it more difficult to marry to the anode voltage of the preceding stage. Level shifting can of course be used (section 13.3.5), but if a direct connection is wanted then this will usually demand pentodes or low-r_a triodes to get the anode voltage low enough. Even then, the cathodyne will often end up biased on the hot side (i.e. with a high grid voltage) so output swing may be sacrificed. Of course, this doesn't really matter, provided we are left with enough available swing to drive the following stage.

For example, the upper image in fig. 12.18 shows a loadline for a gain stage using an ECC88 with a 250V HT. The load impedance is 68kΩ which is relatively large for such a low-r_a triode, and we will bias it as hot as we dare, to pull the anode voltage down low while avoiding the region of grid current. A cathode load line of 680Ω has been drawn and indicates a bias voltage of about −1.9V and an anode voltage of about 65V. This will therefore be the grid voltage of the cathodyne, hence its

cathode voltage will also be very close to this value. In other words, we now know approximately 65V will be dropped across each of the cathodyne's load resistors, leaving a healthy 120V across the valve itself.

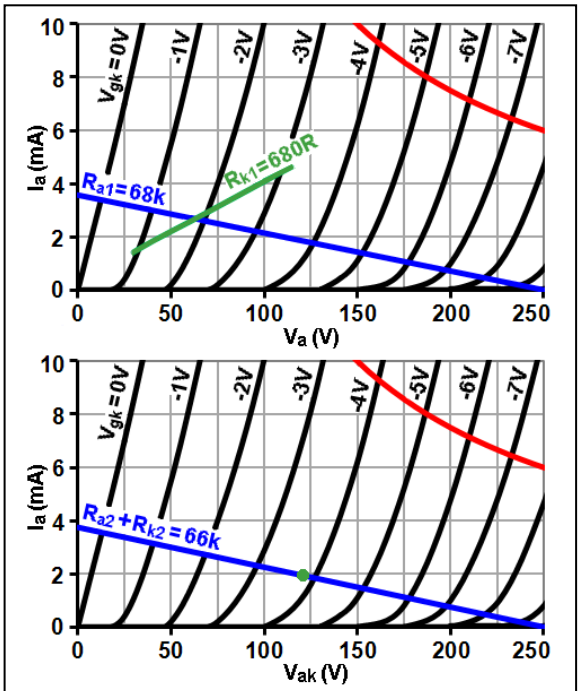


Fig. 12.18: **Upper:** Load line for V_1 in fig. 12.19. **Lower:** Load line for V_2 in fig. 12.19.

The lower image in fig. 12.18 shows the load for line for the cathodyne. Load resistors of 33kΩ have been chosen, i.e. the total load is 66kΩ. With an estimated 120V *across the valve* (the horizontal axis has been labelled V_{ak} for emphasis), as indicated by the dot, the bias voltage will be around −3.8V. The total output swing appears to be about $110V_{pk}$, i.e. $55V_{pk}$ from each output, but in fact this is constrained by the hot-biased first stage which will clip first. Fig. 12.19 shows the completed circuit with obligatory arc protection diode and actual measured voltages. Fig 12.21 shows the distortion measured at the cathode of V_2, which is similar to fig. 12.18 earlier. With C_{k1} fitted the gain was 28.3, falling to 21.4 when removed.

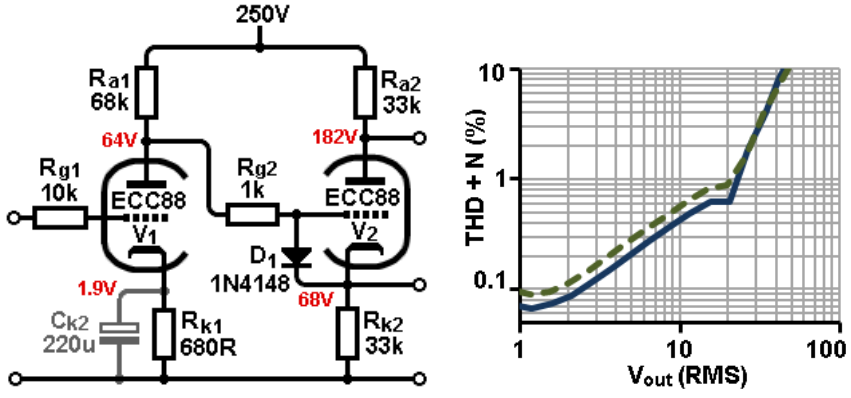


Fig. 12.19: **Left:** Practical direct-coupled cathodyne. **Right:** Distortion performance at 1kHz. **Solid:** V_1 degenerated; **Dashed:** V_1 bypassed.

Apart from demonstrating a perfectly reasonable circuit, there was an ulterior motive for using the particular component values in the previous example: they were taken from a real push-pull amplifier. However, while the circuit works well with an ECC88 the amplifier in question actually used a 6H3П / 6N3P, and this serves to demonstrate a trap that is easily fallen into when DC coupling. After substituting this valve into the previous circuit (it is not pin compatible with the ECC88, by the way) fig. 12.20 shows the 68kΩ load line for the first stage together with its 680Ω cathode load line. These indicate a hotter bias of about −1.5V but a *higher* anode voltage of about 90V, owing to this valve's much lower perveance. We should therefore expect about 90V across each of the cathodyne's load resistors, leaving only about 70V across the V_2 itself.

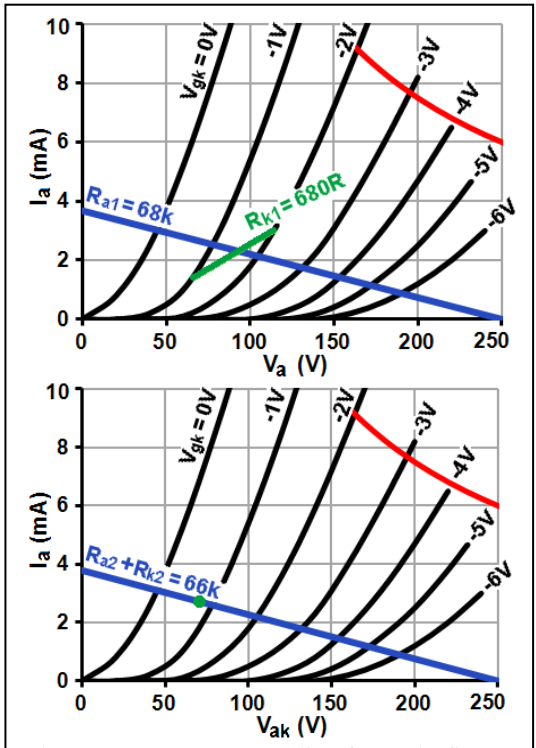
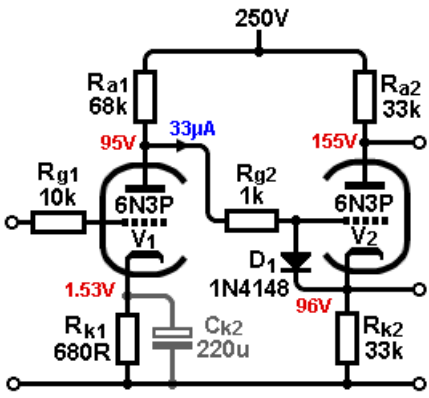


Fig. 12.20: **Upper:** Load line for V_1 in fig. 12.21. **Lower:** Load line for V_2 in fig. 12.21.



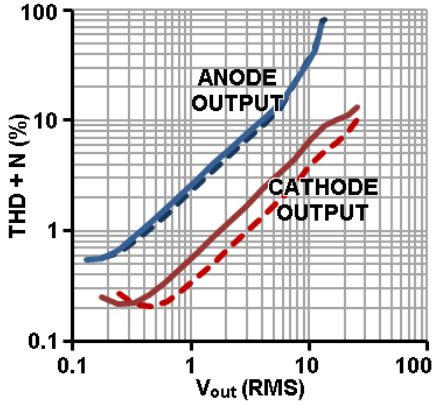


Fig. 12.21: **Left:** Badly conceived direct-coupled cathodyne suffers grid current. **Right:** Distortion performance at 1kHz. **Solid:** V_1 degenerated; **Dashed:** V_1 bypassed.

Fig. 12.20 also shows the load line for the cathodyne and, with the predicted bias point indicated by the dot, the resulting bias is smaller than −1V so we are within the region where grid current might flow. Fig. 12.21 shows the circuit with actual measured voltages, and by measuring the voltage across R_{g2} it was found that about 32µA does indeed flow into the grid of V_2 at idle. Now when the anode voltage of V_1 swings down, grid current will fall, and when it swings up it will increase, i.e. the input resistance of V_2 will vary (non-linearly) with signal amplitude. This in turn leads to dissimilar outputs and excessive distortion, as demonstrated by the dismal distortion plots. Notice that degenerating V_1 makes the distortion *worse* because it raises the output resistance of V_1 and therefore exacerbates the interaction with V_2's variable input resistance. In other words, this circuit is badly designed –there simply isn't enough HT voltage available for direct coupling to work with this valve type; level shifting, AC coupling, or a different valve should have been used instead.

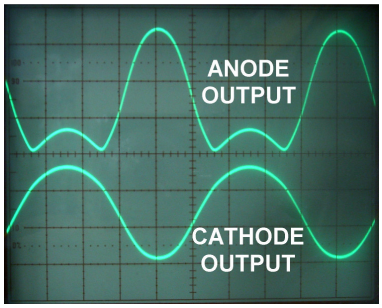


Fig. 12.22: Oscillogram showing the frequency-doubling effect when a cathodyne is heavily overdriven.

But there's more. When the anode of V_1 swings up, driving grid current into V_2, that current flows out of the cathode and down R_{k2}. Eventually V_2 cannot turn on any harder, but the voltage across R_{k2} continues to be 'jacked up' by grid current. With the voltage across the valve unable to shrink further, the anode voltage must therefore be jacked up too, so a copy of the cathode voltage signal peak appears at the anode, resulting in a kind of frequency doubling or full-wave rectification effect. This can be seen in the oscillogram in fig. 12.22 which was produced by the circuit in fig. 12.21 with a $1V_{rms}$ input (V_1 bypassed). This interesting effect is a rare case where harmonic distortion can approach one hundred percent.* It also demonstrates the value of testing an amplifier well beyond its normal 'linear' range –it can reveal bad behaviour that is not obvious on small signal testing, especially if you don't have access to a distortion analyser.

Before finishing this section it is worth mentioning again that although the cathodyne is an exemplary phase inverter, it is unsuitable as a balanced line driver. When sending balanced signals down cables, the *unbalanced* source impedances must be equal if we want good rejection of interfering signals (that is the point of balanced signal transmission, after all). The cathodyne fails this criterion miserably; it would allow far more interference to couple to the anode-driven output, which would not be rejected by the CMRR of the receiving circuit at the far end of the cable. In other words, the cathodyne needs to be buffered from the outside world. This is easy enough to do, but it is perhaps disappointing that the cathodyne's two outputs idle at different DC voltages, so they cannot be directly coupled to a pair of

* The 'distortion' of a perfect square wave is 48.3%, so it is very rare to encounter figures higher than this in even the most egregious audio circuit.

identical cathode followers, say. However, it is worth observing that the cathodyne always hovers exactly half-way between the power-supply rails, so it is possible to level-shift the two outputs to exactly half the total HT voltage while still maintaining perfect balance and symmetry, as illustrated in fig. 12.24. Here the anode output is shifted down to HT/2 by the potential divider R_1/R_2, while the cathode output is shifted up to the same voltage with an identical divider $R_3/R4$, but returned to the HT. They must of course use large resistances to avoid stealing excessive current from the valve. R_1 and R_3 may also be bypassed with capacitors to avoid attenuating AC signals or to compensate for Miller capacitance.

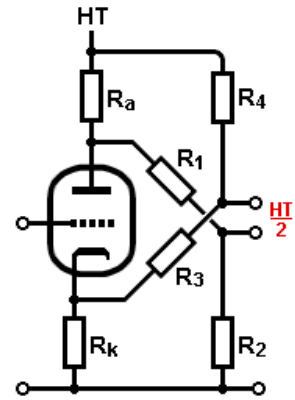


Fig. 12.23: With suitable choice of $R_1/R_2 = R_3/R_4$, the two outputs can be shifted to the same DC voltage of HT/2.

12.3: Appendix:

12.3.1: Input resistance:

Referring to the equivalent circuit in fig. 12.24 and working clockwise around the input mesh:

$$v_{in} = i_{in}R_g + i_{in}R_k - i_{out}R_k$$

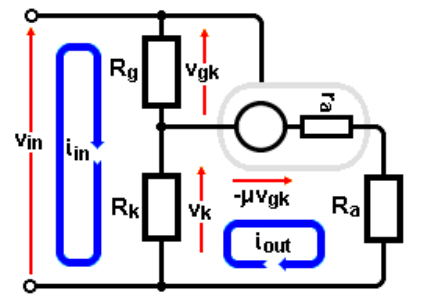


Fig. 12.24: Finding the input resistance of the cathodyne.

For the output mesh:

$$i_{out} = \frac{-\mu v_{gk} + i_{in}R_k}{r_a + R_a + R_k}$$

$$i_{out} = \frac{i_{in}(-\mu R_g + R_k)}{r_a + R_a + R_k}$$

By substituting this into the earlier expression for v_{in}:

$$v_{in} = i_{in}R_g + i_{in}R_k - i_{in}\frac{-\mu R_g + R_k}{r_a + R_a + R_k}R_k$$

We are now in a position to divide both sides by i_{in} and so find the input resistance:

$$R_{in} = \frac{v_{in}}{i_{in}} = R_g + R_k + \frac{\mu R_g R_k - R_k^{\,2}}{r_a + R_a + R_k}$$

$$R_{in} = R_g + R_k + \frac{\mu R_g R_k}{r_a + R_a + R_k} - \frac{R_k^{\,2}}{r_a + R_a + R_k}$$

But the first fraction contains an expression for the open-loop gain A_o, which can then be put in terms of the closed-loop gain (to the cathode) A_k:

$$\frac{\mu R_k}{r_a + R_a + R_k} = A_o = \frac{A_k}{1 - A_k}$$

Hence:

$$R_{in} = R_g + R_k + R_g \frac{A_k}{1 - A_k} - \frac{R_k^{\,2}}{r_a + R_a + R_k} \approx R_g \frac{A_k}{1 - A_k}$$